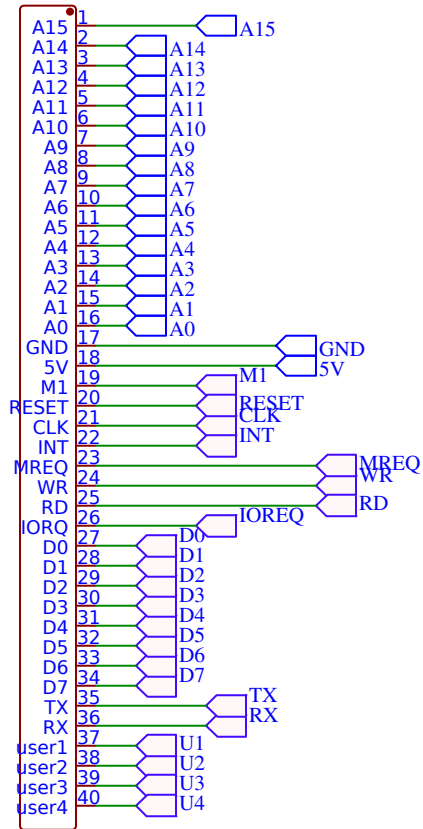
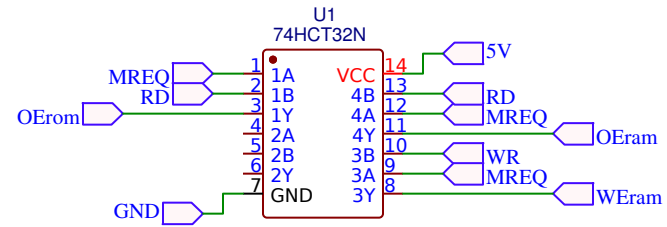
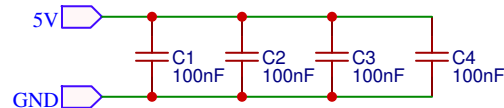
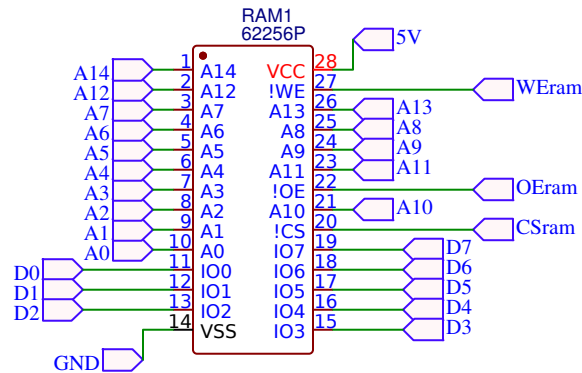


Page ROM to first 32kb and RAM to last 32kb.

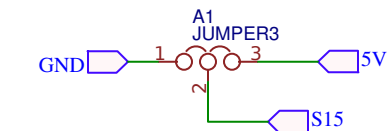
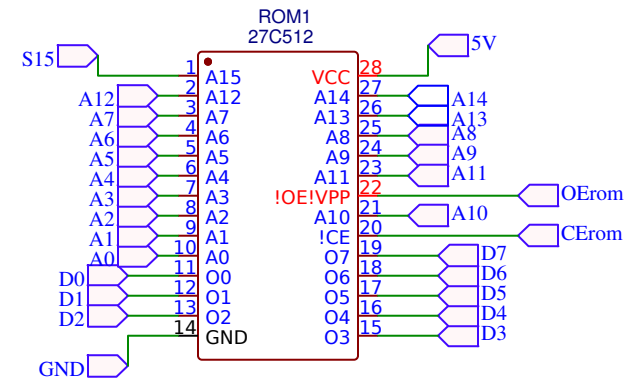
RC2014_BUS
2.54mm 1x40P



A14 5V
A12 !WE
A7 A13
A6 A8
A5 A9
A4 A11
A3 !OE
A2 A10
A1 !CS
A0 D7
D0 D6
D1 D5
D2 D4
GND D3



A15 5V
A12 A14
A7 A13
A5 A8
A6 A9
A4 A11
A3 !OE
A2 A10
A1 !CS
A0 D7
D0 D6
D1 D5
D2 D4
GND D3



Split 64kb ROM in two sections
upper and lower

TITLE: 44 ROM+RAM 32k banks		REV: 1.0
Date: 2018-07-15	Sheet: 1/1	
EasyEDA V5.6.10	Drawn By: karlab	